CURRENT SOURCES, CURRENT SINKS AND CURRENT MIRRORS

1 Introduction:

Current sources and current mirrors form one of the most important components in Analog Circuits. When a source of current flows from the highest positive potential (V_{DD}) into a load it is designated a current source while when the source of current flows from the load to the ground, it is designated a current sink. A schematic of a current source and a current mirror is shown in Fig. 1. A simplest current source/sink can be constructed using a fixed gate voltage to a P-MOS Transistor / N-MOS Transistor respectively. When a P-MOS Transistor is used with a fixed gate voltage V_{GG} to obtain a current source, we will get a near constant current so long as the transistor is in saturation, i.e so long as the source to drain voltage $V_{SD} \leq V_{SG} + \left|V_{TH}^{P}\right|$. Similarly for a current sink with N-MOS Transistor the drain to source voltage $V_{DS} \leq V_{GS} + V_{TH}^{N}$ we will get a near constant current. The voltage V_{SD} and V_{DS} for the P and N Transistors respectively represent the voltage across the current source and sink respectively. The minimum voltage magnitude across the source/sink defines one of the important characteristics of the current

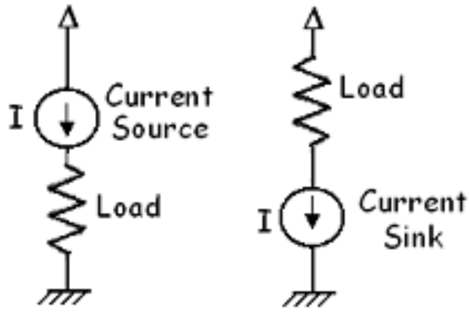
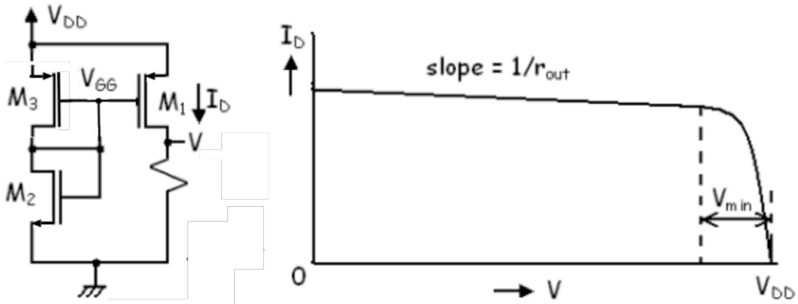
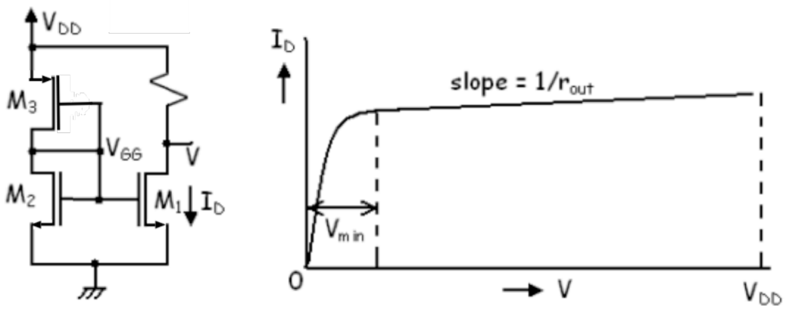


Fig. 2.1 Definition of Current Source and Sink.



a) Current Source



b) Current Sink

Fig.2 Basic characteristics of a current source and a sink.

source/sink (see Fig. 2), the other characteristics of interest is the reciprocal of the slope of the I-V curve in the region of near constancy of output current, the output impedance r_{out}. In the Current source/sink circuits shown in Fig. 2, the role of the diode connected transistors is to provide the necessary bias voltage V_{GG}. The required V_{GG} can be obtained by choosing the appropriate sizes for M_1 and M_2. Before proceeding to evaluate the output impedance and identify methods to improve r_{out}, let us recollect the equivalent circuit of an NMOS transistor.

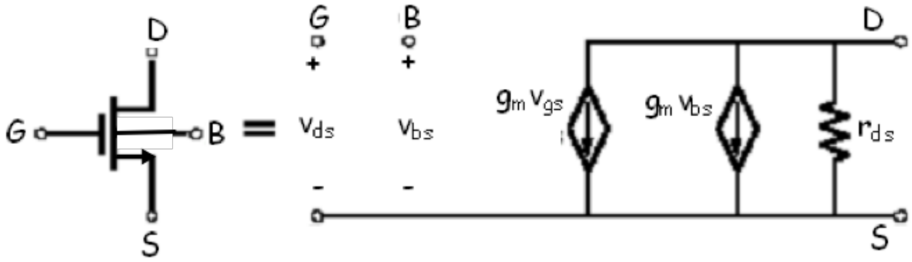


Fig. 3 Equivalent circuit of a NMOS Transistor.

It is evident that the output impedance of both the current source and the sink are r_{ds} of the output transistor that acts as the constant current source/sink. Before proceeding further it is essential to obtain an answer to the question of how do we obtain the exact value of V_{GG} required to obtain a designated value for the current source/sink. Since it involves the proper sizing of the M and P transistors it raises the question about how accurate can it get to be. An interesting way around this problem is to replace M_2 in Fig. 2(a) with a current sink of required current value and retain M_3 as a diode connected P Transistor and replace M_3 in Fig. 2(b) with a current source of required current value and retain M_2 as a diode connected N Transistor as shown in Fig. 4.

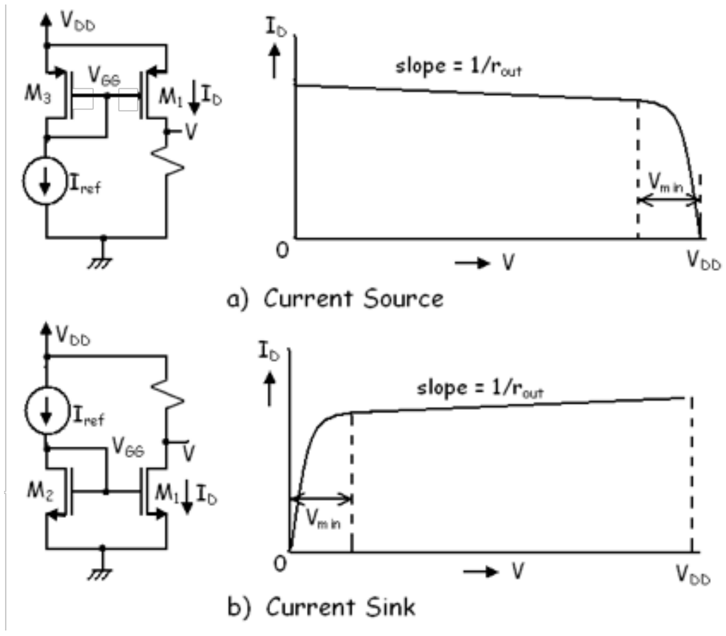


Fig. 4 Modified current source and sink of Fig. 2.

The configuration of current source and sink given in Fig. 4 are called Current Mirrors. A name derived from the fact that the gate to source voltage of M_1 and M_3 in Fig. 4(a) and the gate to source voltage of M_1 and M_2 ensures that M_1 mirrors the current $I_{ref.}$ This configuration of current mirror is also called the Simple Current Mirror.

Sources of error in a simple Current Mirror:

Fig. 5 represents the operative part of a simple current mirror shown earlier. Let us now look in to the sources of error in the mirroring action of M_1 of I_{ref} flowing in M Assuming that both the transistors are in saturation, we can write the ratio of currents I_{out}/I_{ref} as

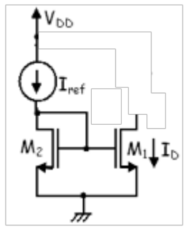


Fig. 5 Simple Crrrent Mirror

$$\frac{I_{out}}{I_{ref}} = \frac{\beta_1}{\beta_2}\left(\frac{(V_{GS1} - V_{TH1})^2}{(V_{GS2} - V_{TH2})^2}\right)\left(\frac{(1+\lambda V_{DS1})}{(1+\lambda V_{DS2})}\right) \qquad (1)$$

With $V_{GS1} = V_{GS2}$ by connection, if the two transistors are perfectly matched,

$$\frac{I_{out}}{I_{ref}} = \frac{W_1 L_2}{W_2 L_1}\left(\frac{(1+\lambda V_{DS1})}{(1+\lambda V_{DS2})}\right) \qquad (2)$$

that reduces to (W_1L_2/W_2L_1), if V_{DS1} equals V_{DS}

2 Configurations of Current Mirrors:

The simple current mirror shown in Fig. 4 has an output impedance limited to r_{ds}. In this configuration, V_{min} is determined by the drain voltage required to ensure that the transistor M_1 is in saturation for a gate voltage V_{GG} i.e $V_{min} = V_{GG} - V_{TH}$. Furthermore, the drain to source voltage of the mirroring transistor V_{DS1} will depend on the load and hence the mirroring action. Various modifications have been suggested to the simple current mirror configuration to improve some or all of he above features. We will now look in to some of the configurations to obtain as good a current mirror as possible, i.e with a low V_{min}, a large output impedance and as good a mirroring as possible ($V_{DS1} \approx V_{DS2}$).

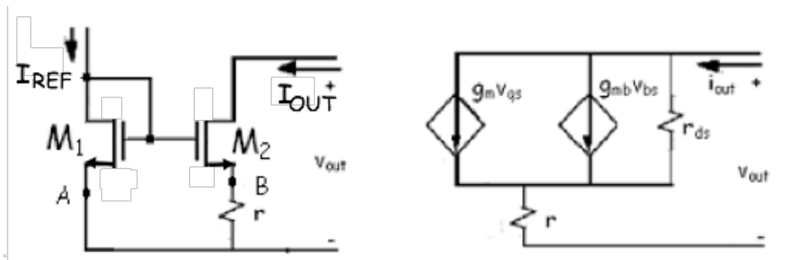


Fig. 6 A Current Mirror with a source resistance (a) the circuit (b) the small signal equivalent circuit.

Fig. 6 shows a current mirror with a source resistance to improve the output impedance. From the equivalent circuit we can write

$$v_{out} = \left[i_{out} - \left(g_m v_{gs} + g_{mb} v_{sb} \right) \right] r_{ds} + i_{out} r \tag{3}$$

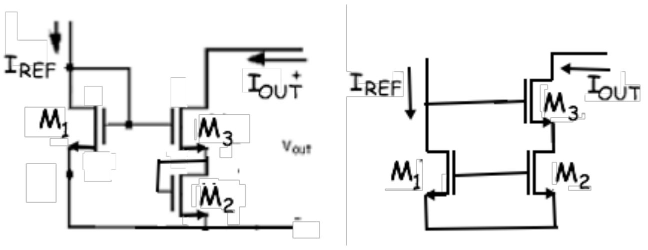
and
$$r_{out} = \frac{v_{out}}{i_{out}} = r_{ds} + r\left(g_m r_{ds} + g_{mb} r_{ds} + 1 \right) \approx \left(g_m r \right) r_{ds} \tag{4}$$

We see that by the introduction of a resistance in the source lead, we obtain output impedance increased by a factor $g_m r$. In the presence of the resistance r, the reflected current in M_2 is also modified. We now have

$$I_{OUT} = \frac{K_N}{2} \left[(V_{GS2} - V_{TH}) \right]^2$$

where $V_{G2}=V_{G1}-(I_{OUT})r$, reducing the mirrored current. This is a very useful configuration to obtain lower current in the mirroring branch. This configuration was very popular during design with Bipolar Transistors for low current design.

2.1. Wilson Current Mirror:



(a) (b)

Fig. 7 Development of Wilson Current Mirror.

Fig.7a shows a modification of Fig. 6 with resistance r replaced with a MOD diode for increasing the output impedance. However as said earlier it reduces the magnitude of mirrored current. A further modification is done as in Fig. 7(b) to mirror the current completely. This circuit is called a Wilson current mirror. From the equivalent circuit of the circuit in Fig. 7(b) we can obtain the output impedance of the Wilson current mirror as

$$r_{out} = \frac{r_{ds1} g_{m2} r_{ds2} g_{m3} r_{ds3}}{r_{ds1} g_{m1}} \approx r_{ds2} \left(g_{m3} r_{ds3} \right) \quad if\ g_{m1} = g_{m2} \tag{5}$$

This modification to the Simple Current mirror does ensure an increased output impedance, but does not ensure $V_{DS1} = V_{DS2}$. V_{min} obtained in this configuration is the sum of the voltage, $V_{DS1}(sat)$ and $V_{DS3}(sat)$, the minimum drain to source voltage required to keep M3 and M1 in saturation. Defining $V_{ON} = V_{GS} - V_{TH}$, and assuming that all transistors have same W/L ratio, we have $V_{DS1} = V_{GS1} = V_{ON} + V_{TH}$ and $V_{DS3}(min) = V_{ON}$ and $V_{min} = 2V_{ON} + V_{TH}$. To ensure that the V_{DS} of the gate tied transistors M_1 and M_2 to be equal we introduce another transistor M_4 in series with M_1 as shown in Fig. 8.

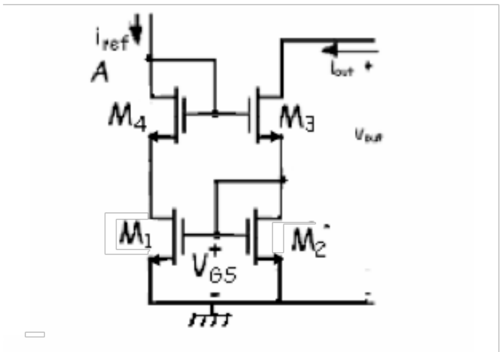


Fig8 Modified Wilson Current Mirror

The circuit in Fig. 8 is called the Modified Wilson Current Mirror. The potential at point A, assuming that all transistors have identical W/L ratios, will be $2V_{GS}$. It is evident from the circuit that with the gate to source voltage of M_4 being V_{GS}, the V_{DS} of M_2 will also be V_{GS} as in M_1. The output impedance and V_{min} of the modified current mirror is the same as Wilson current mirror.

2.2. Cascode Current Mirror:

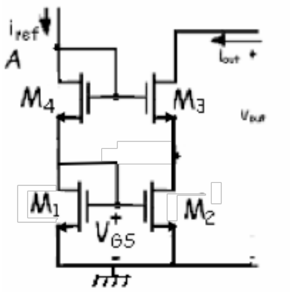


Fig. 9 Cascode Current Mirror.

In Fig. 5, including a source resistance in the mirroring circuit modified the simple current mirror. Instead, if we insert another mirror pair in series with a simple current mirror, we obtain a cascode current mirror shown in Fig. 9. In the cascode current mirror, if we choose W/L ratios of all the transistors equal, we have the potential at A equal to $2V_{GS}$. With the gate to source voltage of M_4 being V_{GS} the voltage at C and hence V_{DS} of M_1 will also be V_{GS} thus giving a very good mirroring. The output impedance in this case will also be given by eqn. 3. In a cascode current mirror, with the gate of M_2 being at $2V_{GS} = 2V_{ON} + 2V_{TH}$, we obtain $V_{min} = 2V_{ON} + V_{TH}$.

2.3. Regulated Cascode Current Mirror:

In Fig. 10 we present the development of a high output impedance current mirror called the regulated Cascode Current Mirror from Wilson Current Mirror. In Fig. 10 (a) we have the normal Wilson Current Mirror that has been recast as in Fig, 10(b). If we dis connect the gate of M_1 from the source and apply a potential V_{GS}, the circuit will be functionally the same but with a different output impedance. It is evident, comparing the circuit with the circuit shown ibn Fig.5, in the Wilson current mirror the value of R realised is $1/g_m$ while for the modified circuit in Fig. 10(c) it will be the drain to source impedance. Fig. 10(d) presents the complete circuit with V_{GS} for M_1 generated through another branch using the principle of a current mirror. While V_{min} and the matching of V_{DS} for good mirroring is same as in an improved Wilson current mirror, the output impedance will be different. It can be easily obtained from the equivalent circuit that the output impedance of Regulated Cascode Current Mirror will be

$$r_{out} = r_{ds3} + r_{ds2}\left(1 + r_{ds3}\left(g_{m3} + g_{mb3}\right)g_{m1}\, r_{ds1}\, g_{m3}\, r_{ds3}\right)$$
$$\approx r_{ds2}\, g_{m1}\, r_{ds1}\, g_{m3}\, r_{ds3} \qquad (6)$$

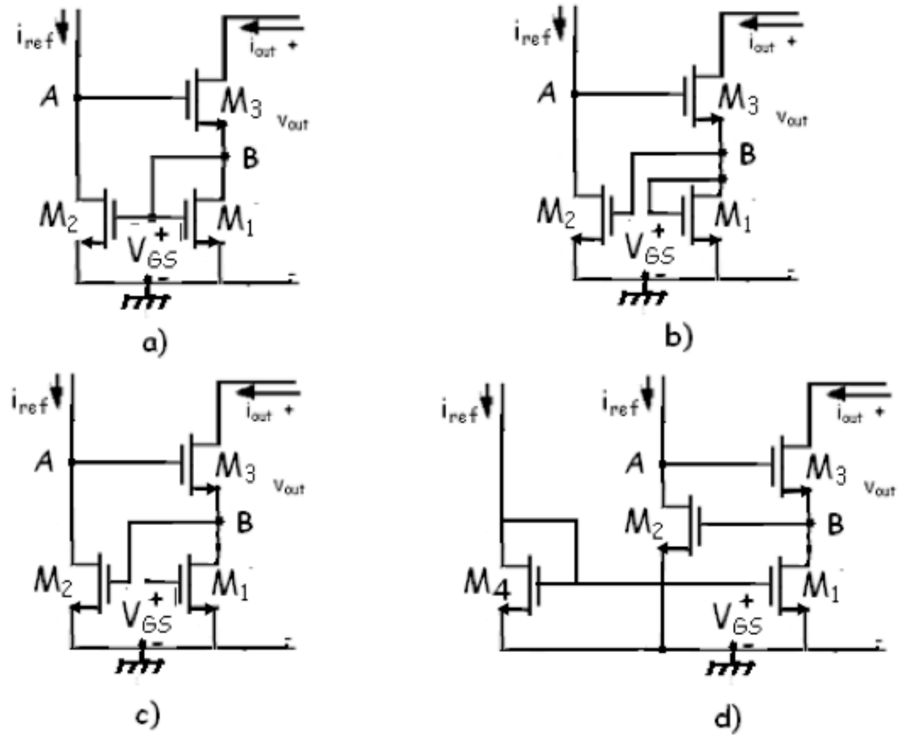


Fig. 10 Development of Regulated Cascode Current Mirror

We see that in a Regulated Cascode Mirror the output impedance is increased by a factor $g_{m1}r_{ds1}$. We see from Fig. 10(d) that if all transistors have the same size, $V_{GS2} = V_{DS1} = V_{GS} = V_{DS4}$, giving us a very good match in mirroring.

We have so far looked in to approaches that could give us high output impedance. Let us now consider a few modifications to get a good match and a low V_{min} with reasonably high output impedance with some modification to the cascode structure.

2.4. Current Mirror with low V_{min} and good mirroring property.

Fig. 11 represents the schematic structure of a Cascode Current Mirror. We see that in the Cascode Current Mirror in Fig. 2.9, the voltage V_{GG2} was obtained as $2V_{GS}$ and hence we had a V_{min} of $2V_{GS} - V_{TH} = 2V_{ON} + V_{TH}$. However if we can obtain $V_{GG2} = 2V_{ON} + V_{TH}$, V_{min} can be reduced to $2V_{ON}$. This can be achieved by introducing another branch with i_{ref} current as shown in Fig. 2.11. A scheme to implement this to obtain a lower $V_{min} = 2V_{ON} + V_{TH}$ is shown in Fig. 2.12. Here we have introduced

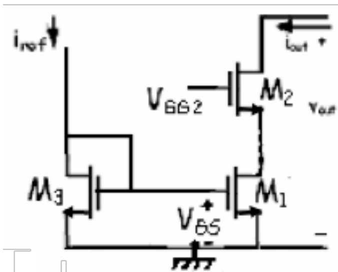


Fig. 11 Schematic of a basic Cascode Current Mirror

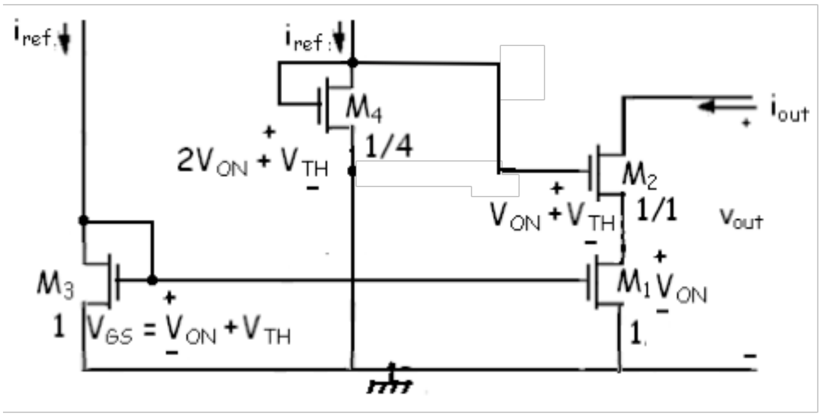


Fig. 12 A scheme to improve the V_{min} of the current mirror.

another current branch containing MOS transistor M_4 with a W/L ration $\frac{1}{4}$ of all other transistors. This is done at a cost of a slight mismatch in the mirroring as $V_{DS3} \neq V_{DS1}$ while $V_{GS3} = V_{GS1}$. A matching can be obtained if we can modify the branch containing M_3 to obtain $V_{DS3} = V_{ON} = V_{DS1}$. A circuit incorporating this is shown in Fig. 2.13 wherein we have added an additional transistor M_5 to achieve this. We can see from the figure that the V_{min} achievable with this circuit is $2V_{ON}$. This circuit is called Wide Range Cascode Current Mirror.

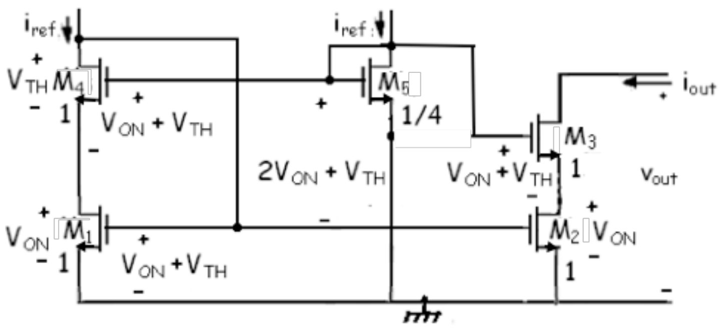


Fig. 13 Wide range Cascode Current Mirror.

We summarize the salient properties of all the current mirrors in the table below.

Current Mirror	Accuracy	Output impedance	V_{min}
Simple	Poor	r_{ds}	V_{ON}
Wilson	Poor	$g_m r_{ds}^2$	$2V_{ON} + V_{TH}$
Improved Wilson	Excellent	$g_m r_{ds}^2$	$2V_{ON} + V_{TH}$
Cascode	Excellent	$g_m r_{ds}^2$	$2V_{ON} + V_{TH}$
Regulated Cascode	Good	$g_m^2 r_{ds}^3$	$2V_{ON} + V_{TH}$
Wide Range Cascode	Excellent	$g_m r_{ds}^2$	$2V_{ON}$